2 ADC, 8 DAC, 96 kHz, 24-Bit Σ-Δ Codec

Silicon Anomaly Sheet — AD1837

This document details known bugs in the current version of the AD1837.

Analog Devices, Inc. is committed, through future silicon revisions, to continuously improve silicon functionality.

The bugs described in this document have been fixed in the A version of this part (AD1837A).

Analog Devices, Inc. will use its best endeavors to ensure that these future silicon revisions remain compatible with your present software/systems implementing the recommended workarounds outlined in this document.

ADC Phase Shift Bug

The ADC engine used in the AD1837 loads the serial port with the results of the last conversion periodically at the sample rate. The loading operation is initially determined by where the $\overline{PD}/\overline{RST}$ pin goes high. For slave mode operation, the loading operation and LRCLK or FSTDM signal have no fixed relationship so it is possible that the loading operation can occur in the middle of a data transfer. This results in the right ADC sample being one sample ahead of the left ADC sample, which presents itself as a phase shift. See Figure 1.

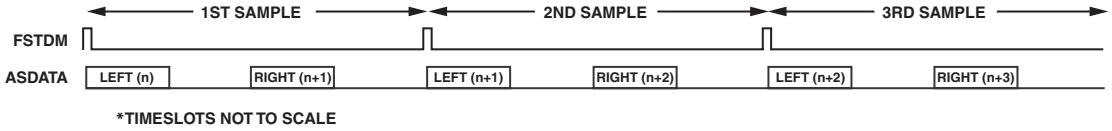

Figure 1. Phase Shift Bug

Workaround

Synchronizing the rising edge of $\overline{PD}/\overline{RST}$ with the appropriate LRCLK (for I^2S, left or right justified modes) or FSTDM (for TDM256 mode) edge will ensure that the ADC result updates occur in a safe region and the phase shift will not occur. Figure 2 shows a synchronization circuit using a single flip-flop that latches the reset signal on the rising edge of FSTDM/ALRCLK. Figure 3 shows an alternate circuit for latching the reset on the falling edge of ALRCLK. Figure 4 shows a timing diagram associated with Figure 2. Table I lists the ADC modes affected by this issue and which circuit should be used to prevent it occurring.

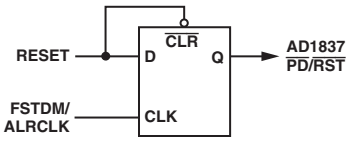

Figure 2. Synchronization Circuit for Rising Edges

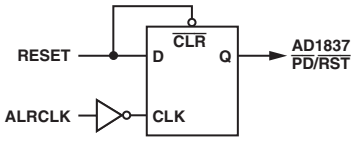

Figure 3. Synchronization Circuit for Falling Edges

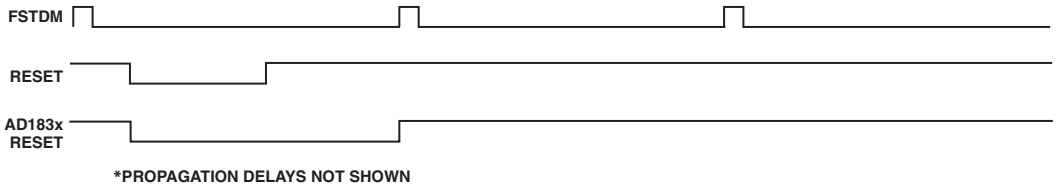

Figure 4. Reset Synchronized to Rising Edge of FSTDM/ALRCLK

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Table I. Safe Regions for $\overline{PD}/\overline{RST}$ Rising Edge

ADC Mode	Safe Region	Recommended Circuit
I^2S	On rising edge of ALRCLK	Figure 2
Left Justified	On falling edge of ALRCLK	Figure 3
Right Justified	On rising edge of ALRCLK	Figure 2
TDM256	On rising edge of FSTDM	Figure 2

96 kHz Operation
When it is required to operate the AD1837 in 96 kHz mode, two write operations are required to the SPI registers to program the IMCLK divider and the ADC sample rate. Programming these two registers can also cause the phase shift error.

Workaround
To guarantee proper operation, programming these registers should occur during the internal reset time. The internal reset time is 3072 MCLK periods from the rising edge of $\overline{PD}/\overline{RST}$ (approximately 12 sample intervals).

ADC Power-Down via SPI Register
Powering the ADCs down and then back up will cause the ADC engine to begin updating the ADC results periodically at the sample rate. Since SPI writes are typically asychronous to the ADC FSTDM/ALRCLK signals, it is possible that the updates can occur in a region that will cause the previously described phase shift issue. It is therefore recommended that the ADC power-down bit not be used when the AD1837 ADC is operated in slave mode.

TDM256 Master Mode—ADC Section
When the AD1837 is operated in TDM256 master mode, the phase shift error is always present. Since the AD1837 generates the FSTDM signal after a reset, it is not possible to synchronize these two signals.

Workaround
Since no data is actually lost, the phase relationship can be reestablished in the DSP or other controller under software control.

DAC Writes
When a write to one of the DAC registers is generated, an internal strobe pulse is used to indicate that the write is finished and the contents of the serial shift register can be loaded to the DAC register. On rare occasions the relationship between the rising edge of CLATCH and the MCLK can cause this pulse not to be generated and the write to the register is ignored.

Workaround
Writing the same value to the DAC twice will ensure that the register gets updated correctly.